Remarks

The Official Action rejected claims 1-32 and 35-37and objected to claims 33 and 34. Applicant has amended claims 1, 13, 15-18, and 25 and canceled claim 14. Claims 1-13 and 15-37 remain pending. Applicant respectfully requests allowance of the pending claims in light of the points that follow.

Examiner Interview and Summary

Applicant gratefully thanks the Examiner for taking the time to discuss the 35 USC § 101 rejections of claims 1, 7-8, 10-11, 25-29, 30-31 and 35-37 during a teleconference held on July 10, 2006. In particular, Applicant thanks the Examiner for explaining the guidelines regarding "a useful and tangible result." Additional details regarding the substance of the interview are presented below in regard to the 35 USC § 101 rejections.

Allowable Subject Matter

Applicant gratefully acknowledges that claims 33 and 34 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant, however, has not elected to rewrite claims 33-34 at this time since Applicant believes the claims from which they depend are also allowable.

Claim Rejections – 35 USC § 101

The Office Action rejected claims 1, 7-8, 10-11, 25-29, 30-31, and 35-37 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Applicant respectfully traverses this rejection in view of the remarks that follow. In

particular, claims 1, 7-8, 10-11 and 30-31 were rejected for lack of producing a useful and tangible result and claims 25-29 and 35-37 were rejected for being directed to descriptive material per se.

Claims 1, 7-8, 10-11 and 30-31

Applicant respectfully disagrees with the Official Action regarding whether claims 1, 7-8 and 10-11 lack a useful and tangible result. However, in the interest of expediting prosecution, Applicant has amended claim 1 to include storing instrumentation data as discussed with the Examiner during the teleconference of July, 10, 2006. Applicant thanks the Examiner for indicating that adding "storing" to claim 1 should overcome the present rejection of claims 1, 7-8, 10-11 and 30-31. Applicant respectfully requests the withdrawal of the present rejection.

Claims 25-29 and 35-37

Applicant has amended claim 25 to include a processor to execute modules of the apparatus. Again, the Applicant thanks the Examiner for indicating that the addition of a processor to claim 25 should overcome the present rejection of claims 25-29 and 35-37. Applicant respectfully requests the withdrawal of the present rejection.

Claim Rejections – 35 USC § 102 (Bargh)

The Official Action rejected claims 1 and 13 under 35 USC 102(e) as being anticipated by Bargh et al (US 6,195, 627). Applicant respectfully requests the rejection of claims 1 and 13 to be withdrawn.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even

one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claims 1 and 13

Claims 1 and 13 require having the **logic design element automatically collect** and store **instrumentation data during the simulation,** wherein the instrumentation data **represents usage and performance related statistics** that relate to the logic design element. The Official Action appears to rely on Figs 4A and 4B and the description provided in col. 12, lines 25-67; cols.13-14 of Bargh to teach the limitations of claims 1 and 13.

Bargh discloses (in Abstract section) that a design entity, which is a part of the logic design is first described and then an instrumentation entity designed to detect occurrences of the design entity is described. However, Bargh indicates that design entity is monitored by the instrumentation entity without the instrumentation entity becoming incorporated into the digital design circuit. Bargh discloses (as described in col. 12, lines 33-40 and 49-54) a simulation model comprising "design entities" and "instrumentation entities". An instrumentation entity is associated with a design entity referred to as target entity. Instances of instrumentation entities are created and connected to the target entities within the simulation model. However, the instrumentation entity and target entity are two distinct entities and the instrumentation entity is not incorporated into the design entity.

Incorporating an instrumentation entity into the logic design may offer challenges, the solution of which are not taught by Bargh. Thus, Bargh does not teach each and every limitation taught by the claims 1 and 13. Since, Bargh does not teach every

limitation of claims 1 and 13, Bargh does not anticipate the invention of claims 1 and 13. Applicants respectfully request the rejection of claims 1 and 13 be withdrawn.

Claim 25

Claim 25 requires "**a collection module that is integrated with the logic design element** and that is structured and arranged **to automatically collect** and store **instrumentation data, which represents usage and performance related statistics relating to the logic design element** during the simulation. The Official Action appears to rely on Fig 4B, element 420, and col. 12, lines 25-67 and col. 13 and 14 to teach the limitations of claim 25.

As described above, simulation model of Bargh discloses "design entities" and "instrumentation entities", which are distinct entities and the instrumentation entity of Bargh does not appear to be integrated with the logic design element to automatically collect instrumentation data relating to the logic design. The block 420 of Fig. 4B appears to be an instrumentation logic block 420 to record occurrences of each type of events of each design entity. The instrumentation logic block 420 appears to be a common space to record the events of each design entity. As depicted in Fig. 4B, the instrumentation logic block 420 appears to be recording the occurrence of events of the instantiations 321a, 321b, and 322.

Thus, Bargh does not appear to teach **a collection module that is integrated with the logic design element** and that is structured and arranged **to automatically collect instrumentation data, which represents usage and performance related statistics relating to the logic design element** during the simulation as required by claim 25. Since, Bargh does not teach every limitation of claim 25, Bargh does not

anticipate the invention of claim 25. Applicants respectfully request the rejection of claim 25 be withdrawn.

Claim Rejections – 35 USC § 102 (Watkins)

The Official Action rejected claims 1-6 and 13-18 under 35 USC 102(b) as being anticipated by Watkins et al (US 5,220,512). Applicant respectfully requests the rejection of claims 1-6, 13, and 15-18 to be withdrawn.

Claims 1 and 13

Claims 1 and 13 require having the **logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data represents usage and performance related statistics that relate to the logic design element**. The Official Action appears to rely on Figs 3 and 4 and the description provided in col. 8, lines 4-6; col.1, lines 15-49; col. 5, lines 5-10; col. 10, lines 53-68; and col. 11, lines 1-4 to teach the limitations of claims 1 and 13.

Watkins discloses (in col. 10, lines 53-63 describing Fig. 3) a display screen 300 to display the textual state information, at different points to be monitored, when provided with different input values. Also, Watkins discloses (in col. 11, lines 8-14, describing Fig. 4) a display screen 400 displaying timing diagrams, at different points to be monitored, when provided with different input values. Watkins merely teaches an ECAD system to collect the results (textual or graphical), generated by the logic circuit, at different points to be monitored after providing inputs to the logic circuit. The points to be monitored may correspond to nets 324, 326, 332, and 328 and the results correspond to the output generated at the nets 324, 326, 332, and 328 based on the simulation inputs.

The state information may represent, for example, a list of logic 1's and 0's generated by a logic circuit when provided with test inputs. The state information does not represent usage and performance related statistics that relate to the logic design element as required by the claims 1 and 13. Since Watkins does not teach every limitation of claims 1 and 13, Watkins does not anticipate the invention covered by the scope of claims 1 and 13. Applicants respectfully request the rejection of claims 1 and 13 be withdrawn.

Claims 2-6 and 15-18

Each of claims 2-6 and 15-18, respectively, depend from one of the claims 1 and 13. Accordingly, each of claims 2-6 and 15-18 are allowable for at least the reasons given above. Applicant respectfully request allowance of claims 2-6 and 15-18.

Claim 25

Claim 25 requires **a collection module that is integrated with the logic design element** and that is structured and arranged **to automatically collect instrumentation data, which represents usage and performance related statistics relating to the logic design element** during the simulation. The Official Action appears to rely on Figs 2, 3, element 224 of Fig 2, and the description provided in col. 8, lines 4-6; col.1, lines 15-49; col. 5, lines 5-10; col. 10, lines 53-68; col. 11, lines 1-4; and col. 7, lines 17-27 to teach the limitations of claim 25.

As described above, ECAD system of Watkins enable a user to provide commands to the simulator using a schematic editor and observe the results of simulation that correspond to outputs at the points to be monitored, on the schematic editor. The state information as described above represents the output generated by

the logic circuit when provided with inputs. The Office Action appears to be giving an unreasonably broad interpretation to the term "state information" to include instrumentation data as well. However, the state information collected by Watkins do not represent instrumentation data, wherein the instrumentation data **represents usage and performance related statistics relating to the logic design element.** Since Watkins does not teach every limitation of claim 25, Watkins does not anticipate the invention disclosed in claim 25. Applicants respectfully request the rejection of claim 25 be withdrawn.

Claim 26-27

Each of claims 26-27 depend from claim 25. Accordingly, each of claims 26-27 are allowable for at least the reasons given above. Applicant respectfully request allowance of claims 26-27.

Claim Rejections – 35 USC § 103(a) (Watkins/Sharma)

The Official Action further rejected claims 7-9, 19-21, and 28 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) in view of Sharma (US 5,978,574). Applicants respectfully request allowance of claims 7-9, 19-21, and 28 in light of the points that follow.

Claims 7-9 and 19-21

Claims 7-9 and 19-21 require having a **FIFO memory to automatically collect the instrumentation data** that includes having the FIFO memory automatically collect the instrumentation data during the simulation, **with the instrumentation data relating to the FIFO memory**. The Official Action appears to rely on FIG. 3 and the description

provided in col. 5, lines 5-10, col. 10, lines 53-68, and col. 11, lines 1-4 of Watkins and FIG. 2 and FIG. 3 and the description provided in col. 1, lines 63-67, col. 2, lines 10-14, and lines 31-36 of Sharma to teach the limitations of claims 7-9 and 19-21.

As described above, Watkins does not teach a logic design element that can automatically collect the instrumentation data during the simulation, wherein the instrumentation data represents usage and performance related statistics relate to the logic design element. Sharma discloses that (in col. 2, line 61 through col. 3 line 4) there is a need in the art for a method and apparatus for verification of queue flow control that substantially covers the corner or the worst case situations. However, Sharma indicates that such a method or apparatus would not completely eliminate the need for simulation, emulation and verification. Sharma merely indicates that by reducing the number of bugs, particularly the queue flow control bugs, early in the design flow results in a superior system design potentially a faster time to market.

Sharma does not teach a method or an apparatus comprising a **FIFO memory to automatically collect the instrumentation data** that includes having the FIFO memory automatically collect the instrumentation data during the simulation, **with the instrumentation data relating to the FIFO memory**. Neither Sharma nor Watkins, individually or together, teach all of the limitations of claims 7-9 and 19-21. Thus, even a combination of the two references would not anticipate claims 7-9 and 19-21 of the instant application. Applicant respectfully requests the rejection of claims 7-9 and 19-21 be withdrawn.

Claim 28

Claim 28 depends from claim 25 and is allowable for at least the reasons given above. Applicants respectfully request the rejection of claim 28 be withdrawn.

Claim Rejections – 35 USC § 103 (Watkins/Mitchel)

The Official Action further rejected claims 10-12, 22-24, and 29 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) in view of Mitchell (US 5,646,553). Applicants respectfully request allowance of claims 10-12, 22-24, and 29 in light of the points that follow.

Claims 10-12 and 22-24

Claims 10-12 and 22-24 require having the logic design element automatically collect the set of data values that represents facts about the usage of the logic design element includes having **the tri-state bus automatically collect the instrumentation data during the simulation, with the set of data values relating to the tri-state bus.** The Official Action appears to rely on the description provided in col. 7, lines 12-17 of Watkins and abstract, FIG. 1 and Col. 1 lines 45-50 of Mitchell to teach the limitations of claims 10-12 and 22-24.

As described above, Watkins does not teach a logic design element that can automatically collect the instrumentation data during the simulation, wherein the instrumentation data represents usage and performance related statistics relate to the logic design element. Mitchell teaches (in the abstract and col. 1, lines 45-50) to avoid contention by shutting off each device's output enable early. Shutting off output enable early guarantees that the device no longer drives the line by the time any other device begins to drive the line, while holding the data on the bus until the end of the transfer cycle. To this end, Mitchell discloses activating the enable signal on the leading edge of the bus clock and deactivating the enable signal, at a delayed half phase clock edge, to avoid contention.

Mitchell does not teach about simulation of a tri-state bus and about a logic design element such as the tri-state bus automatically collecting instrumentation data corresponding to the logic design element itself. Neither Mitchell nor Watkins, individually or together, teach all of the limitations of claims 10-12 and 22-24. Thus, even a combination of the two references would not anticipate claims 10-12 and 22-24 of the instant application. Applicant respectfully requests the rejection of claims 10-12 and 22-24 be withdrawn.

Claim 29

Claim 29 depends from claim 25 and is allowable for at least the reasons given above. Applicants respectfully request the rejection of claim 29 be withdrawn.

Claim Rejections – 35 USC § 103 (Watkins/Wong)

The Official Action further rejected claim 30 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) as applied to claims 1-6 and 13-18 above, in view of Wong (K F Wong et al: "Statistics on Logic simulation", 1986, IEEE 23rd Design Automation Conference). Applicants respectfully request allowance of claim 30 in light of the points that follow.

Claim 30

Claim 30 requires a **FIFO memory that automatically collects, during the simulation, the instrumentation data, which represents a degree of fullness of the FIFO memory**. The Office Action appears to rely on Section 5.3 on pages 16-17, Fig.1, and description in page 18 to teach the limitations of claim 30.

As described above, Watkins does not teach a logic design element that can automatically collect the instrumentation data during the simulation, wherein the

instrumentation data represents usage and performance related statistics relate to the logic design element. Wong summarizes, in table. 8, benchmark queue length data and Fig. 1 of Wong represents a distribution curve for a priority queue. Wong teaches some factors which are of importance in the design of hardware based logic simulator. Wong discloses a summary of architecture approaches for achieving high performance logic simulation engines and Wong, also, discloses a software simulator, *lism,* which is used to gather data on the simulation process.

Wong does not appear to disclose **a memory that automatically collects, during the simulation, the instrumentation data, which represents a degree of fullness of the FIFO memory** as required by claim 30. Neither Wong nor Watkins, individually or together, teach all of the limitations of claim 30. Thus, even a combination of the two references would not anticipate claim 30 of the instant application. Applicant respectfully requests the rejection of claim 30 be withdrawn.

Claim Rejections – 35 USC § 103 (Watkins/Srivastava)

The Official Action further rejected claim 32 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) as applied to claims 1-6 and 13-18 above, in view of Srivastava (Mani B. Srivastava et al: "Using VHDL for High-Level, Mixed-Mode system simulation", September 1992, IEEE Design and Test of Computers, Volume 9, Issue 3). Applicants respectfully request allowance of claim 32 in light of the points that follow.

Claim 32

Claim 32 requires a **tri-state bus that automatically collects, during simulation, the instrumentation data, which represents a tri-state bus label and a**

bus error condition corresponding to one or more tri-state bus drivers driving the tri-state bus. The Office Action appears to rely on Page 36, figure 3; Page 35, section VHDL model-simulating package; Page 31, last sentence; and Page 32, first two sentences of Srivastava to teach the limitations of claim 32.

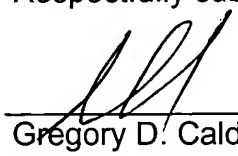
As described above, Watkins does not teach a logic design element that can automatically collect the instrumentation data during the simulation, wherein the instrumentation data represents usage and performance related statistics relate to the logic design element. Srivastava discloses (in page 35) that VHDL template package called MSGPACK_type provides primitives to support system modeling, which allows VHDL processes to communicate using special signals that implement the FIFO, channel-based communication mechanism. Srivastava discloses, in Fig. 3, a VHDL implementation of channels in the process network model. Srivastava appears to teach novel application of VHDL to the modeling of complex and application specific systems. To this end, Srivastava appears to use specialized VHDL packages to model the system's discrete portion as a set of concurrent processes communicating via channels with well-defined protocols.

However, Srivastava does not appear to teach **tri-state bus that automatically collects, during simulation, the instrumentation data, which represents a tri-state bus label and a bus error condition** corresponding to one or more tri-state bus drivers driving the tri-state bus as required by claim 32. Neither Srivastava nor Watkins, individually or together, teaches all of the limitations of claim 32. Thus, even a combination of the two references would not anticipate claim 32 of the instant application. Applicant respectfully requests the rejection of claim 32 be withdrawn.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicants submit that the application is in condition for allowance. Reconsideration is requested, and allowance of the pending claims is earnestly solicited. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities, which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,



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